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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,026	07/11/2003	Seung-Woo Lee	6192.0302.US	2713

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EXAMINER	
MOON, SEOKYUN	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,026	LEE ET AL.	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The Applicants' arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 12-14** are rejected under 35 U.S.C. 102(b) as being anticipated by Lien et al. (US 6,211,851, herein after "Lien")

As to **claim 12**, Lien teaches a method of driving a liquid crystal display including first and second gate lines, a data line, a first pixel connected to the first gate line and the data line, and a second pixel connected to the second gate line and the data line [figs. 2a-2f], the method comprising:

scanning the first gate line ("*G1*");

applying a first data voltage ("*V1*") to the data line during the scanning of the first gate line ("*G1*");

storing the first data voltage applied to the data line during the scanning of the first gate line [fig. 3 and col. 5 lines 40-49];

scanning the second gate line ("*G2*");

applying the stored first data voltage ("*Vm-V1*") [col. 5 lines 23-27] to the data line during the scanning of the second gate line ("*G2*"); and

applying a second data voltage ("*-V2*") to the data line during the scanning of the second gate line ("*G2*").

As to **claim 13**, Lien teaches the method comprising inverting polarity of the stored first data voltage before the application of the stored first data voltage [col. 5 lines 40-49].

As to **claim 14**, Lien [fig. 3] teaches the method comprising buffering the stored data voltage before the polarity inversion.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-4**, **7-9**, **11**, and **15-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 2002/0075214) in view of Lien.

As to **claim 1**, Kim teaches a liquid crystal display [par. (0002) lines 1-2 and par. (0004) lines 3-4] comprising:

a liquid crystal panel assembly including a plurality of gate lines, a data line intersecting the gate lines, and a plurality of pixels connected to the gate lines and the data line [fig. 5];

a signal controller ("*master PCB 200*") receiving image data and a synchronization signal from an external device, processing the image data [par. (0041) lines 3-5] and generating control signals for displaying the image data [par (0041) lines 14-16];

a voltage generator (a combination of "*gray voltage unit*", "*Row driver power generator*", and "*common pulse generator*") generating a plurality of gray voltages and a gate voltage for driving the panel assembly [fig. 1];

Examiner respectfully submits that the Examiner cited the information from Kim's admitted prior art since such components are also included and implemented in Kim's display device.

Kim further teaches:

a gate driver sequentially scanning the gate lines by applying the gate voltage, each scanning being performed in a horizontal period ("*ts*" + "*tm*") including a first period ("*ts*") and a second period ("*tm*") following the first period [fig. 7];

a master data driver ("*master column driver 220*") sequentially applying data voltages selected from the gray voltages corresponding to the image data to the data line, each application is performed in the second period [par. (0051) lines 1-5] [figs. 4 and 7]; and

a slave data driver ("*slave column driver 230*") applying a pre-charging/compensation voltage to the data line in each first period [par. (0051) lines 5-8] [figs. 4 and 7].

Kim does not teach the slave data driver to store the data voltages applied to the data lines and to apply the stored data voltages to the data lines as pre-charging/compensation voltages.

However, Lien teaches a method of storing data voltages of a frame and applying the stored frame data voltages to data lines in a first period of a gate signal period, wherein the gate signal period consists of a first period of applying pre-charging/compensation voltages and a second period of applying image data voltages [col. 3 lines 42-52] [figs. 2a-2f and 3].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kim's slave data driver to apply the pre-charging/compensation voltages to the data

lines by storing image data voltages and applying the stored image data voltages as pre-charging/compensation voltages, as taught by Lien, in order to reduce the crosstalk in Kim's display without increasing the cost or power required to drive pixels included in Kim's display [col. 3 lines 27-29].

As to **claim 2**, Kim modified by Lien [Lien: fig. 2f] teaches that two data voltages sequentially applied to the data line have opposite polarity with respect to a predetermined voltage and the slave driver inverts the polarity of the stored voltage before application to the data line [Lien: col. 3 lines 47-52].

As to **claim 3**, Kim [fig. 4] teaches the master driver ("*master column driver 220*") and the slave driver ("*slave column driver 230*") are disposed at opposite sides of the panel assembly.

As to **claim 4**, Kim modified by Lien teaches the slave driver comprising:

a storage (Lien: "*full frame buffer*") [Lien: fig. 3] for storing the data voltages applied to the data line in the second period; and

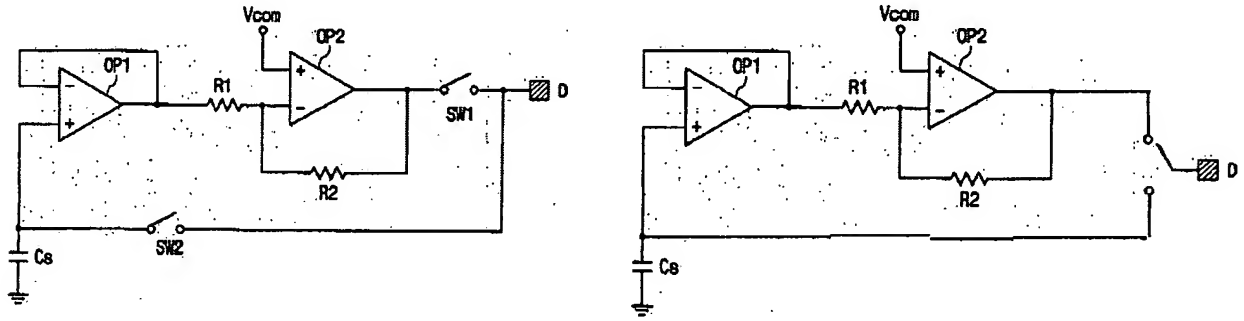
an inverter (Lien: "*inverter 6*") [Lien: fig. 3] for inverting the polarity of the data voltages stored in the storage [Lien: fig. 2f], the storage and the inverter alternately connected to the data line (Lien: "*analog toggle 4*" alternately connects the storage and the inverter to the data lines) [Lien: col. 5 lines 40-49].

As to **claim 7**, Kim modified by Lien [Lien: fig. 3] teaches the slave driver comprising a switch unit (Lien: "*analog toggle 4*") selectively connecting the storage and the inverter to the data line [Lien: col. 5 lines 40-49].

As to **claim 8**, Kim modified by Lien does not expressly teach the switch unit to comprise a first switch and a second switch.

However, since the Applicants have failed to disclose that including two switches in the switch unit provides an advantage, is used for particular purpose, or solves a state problem, it is an obvious matter of design choice to include two switches in the switching unit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a toggle switch for the switching operation of the driver, since a toggle switch would perform equally well at selectively connecting inputs from the storage and the inverter to the data line. Drawing 1 is provided below to illustrate an alternative design/structure for the switching unit.



Design I Design II

Drawing 1

As to **claim 9**, Kim modified by Lien teaches the slave driver to comprise a buffer (Lien: "*full frame buffer*") [Lien: fig. 3] for buffering the data voltage (Lien: "*D1*", "*D2*", "*D3*", ...) stored in the storage and provides the buffered data voltage for the inverter (Lien: "*inverter 6*") [Lien: col. 5 lines 38-49].

Lien does not expressly disclose the buffer to include an operational amplifier.

However, Examiner takes official notice that implementing an operational amplifier to design a buffer is well known and widely used technique.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify the modified Kim's buffer to include an operational amplifier as its component since an operational amplifier is well known for low cost.

As to **claim 11**, Kim modified by Lien teaches the predetermined voltage being applied to the pixels [Lien: fig. 2f].

As to **claim 15**, all of the claim limitations have already been discussed with respect to the rejection of claims 1 and 12.

As to **claim 16**, all of the claim limitations have already been discussed with respect to the rejection of claim 2.

As to **claim 17**, all of the claim limitations have already been discussed with respect to the rejection of claim 4.

As to **claim 18**, all of the claim limitations have already been discussed with respect to the rejection of claim 7.

As to **claim 19**, all of the claim limitations have already been discussed with respect to the rejection of claim 8.

6. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Lien as applied to claims 1-4, .7-9, 11, and 15-19 above, and further in view of Washio et al (US 6,873,313, herein after "Washio").

Kim modified by Lien does not expressly disclose the storage to comprise a capacitor.

However, Washio [figs. 1 and 3] teaches an image display device having a pre-charging unit (a combination of "*pre-charging circuit PC*" and "*pre-charging voltage stabilizing section ST*") comprising a capacitor ("*charging holding means*" shown in fig. 3) to store a pre-charge voltage ("*PCV*") [col. 12 lines 1-20].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the modified Kim's storage to comprise a capacitor, as taught by Washio, since capacitor is well known for low cost and is widely used in a driving circuitry for a display.

7. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Lien as applied to claims 1-4, 7-9, 11, and 15-19 above, and further in view of Lautzenhiser (US 2002/0149503).

Kim modified by Lien [Lien: fig. 3] teaches an inverter (Lien: "*inverter 6*") included in a driving circuitry.

Kim modified by Lien does not expressly disclose the specific structure of the inverter included in the display driver.

However, Lautzenhiser [fig. 21] teaches an inverter ("*inverter 350*") comprising an operational amplifier ("*operational amplifier 354*") in a negative feedback configuration having a non-inverting input terminal supplied with the predetermined voltage ("*ground*") [par. (0223)].

It would have been obvious to one of ordinary skill in the art at the time of the invention to specify the internal structure of the modified Kim's inverter to comprise an operational amplifier in a negative feedback configuration having a non-inverting input terminal supplied with the predetermined voltage, as taught by Lautzenhiser, since including an operational amplifier in a negative feedback configuration to build an inverter is well known and widely used design in analog circuit implementations.

8. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Lien as applied to claims 1-4, 7-9, 11, and 15-19 above, and further in view of AAPA (the Applicants' admitted prior art, herein after "AAPA").

Kim modified by Lien does not expressly disclose the slave driver being formed on the panel assembly.

However, AAPA teaches a master and a slave drivers to be mounted on a liquid crystal panel [Specification: pg 2 lines 19-21].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kim to implement Kim's master and slave drivers on the liquid crystal panel, as taught by AAPA, in order to reduce the size of the display by eliminating the space required to install master and slave drivers.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 22, 2006
S.M.

AMR A. AWAD
SUPERVISORY PATENT EXAMINER